

AMENDMENTS TO THE CLAIMS

1-67. (Cancelled)

68. (Currently Amended) A process for electrochemical deposition of copper onto a surface of a semiconductor workpiece in a plating tool, comprising:

providing a workpiece having a dielectric layer in which recesses have been formed, a barrier layer on the dielectric layer, and a copper seed layer on the barrier layer;

exposing a surface of the workpiece to a plating solution in a plating chamber in the tool, the plating solution including a principal metal species comprising copper to be deposited;

applying plating power between the surface of the workpiece and an electrode electrically coupled to the plating solution to electrolytically deposit copper onto the seed layer and into the recesses, wherein plating power is applied at a first current density for a first period of time to deposit a first amount of copper into the recesses, and subsequently

at a second current density for a second period of time to deposit a second amount of copper onto the first amount of copper to fill the recesses with copper and form a copper overburden extending over the dielectric layer, wherein the second current density is greater than the first current density and a majority of the copper deposited onto the surface of the workpiece is deposited during the second time period, and wherein the second amount of copper has relatively small grain sizes; and

annealing the copper in the recesses and the copper overburden portion at a predetermined elevated temperature while the workpiece is ~~within the tool~~ in an annealing process after filling the recesses with the copper

and before subsequent chemical mechanical polishing processes to increase the grain size of the copper ~~and induce electromigration such that the conductivity of the deposited copper increases and electromigration resistance increases.~~

69. (Previously Presented) The process of Claim 68, wherein the first current density and first period of time are selected to at least partially fill the recesses with the deposited metal.

70. (Previously Presented) The process of Claim 68, wherein copper deposited during the first time period has a grain size that is sufficiently small to fill the recesses and at least some of the recesses have a width of less than or equal to 0.3 micron.

71. (Previously Presented) The process of Claim 68, wherein the metal is annealed at a temperature of below about 250° C.

72. (Currently Amended) The process of Claim 68, wherein the first current density is about 3.2 mA/cm².

73. (Currently Amended) The process of Claim 68, wherein the second current density is about 20 mA/cm².

74. (Previously Presented) The process of Claim 68, wherein a ratio of the second current density to the first current density is about 6:1.

75. (Previously Presented) The process of Claim 68, wherein the first time period is about 30 seconds.

76. (Previously Presented) The process of Claim 68, wherein the metal is annealed at a temperature of below about 300° C.

77. (Previously Presented) The process of Claim 68, wherein metal is deposited at a higher rate during the second time period than during the first time period.

78. (Cancelled)

79. (Cancelled)

80. (Currently Amended) A process for electrochemical deposition of copper onto a surface of a semiconductor workpiece having a dielectric layer, submicron recesses in the dielectric layer, a barrier layer on the dielectric layer, and a copper seed layer on the barrier layer, the process comprising:

exposing a surface of the workpiece to a plating solution in a plating chamber in a tool, the plating solution including copper as a principal metal species to be deposited;

applying plating power between the surface of the workpiece and an electrode electrically coupled to the plating solution to electrolytically deposit copper onto the surface, wherein plating power is applied

at a first current density for a first period of time to deposit a first amount of copper onto the surface of the workpiece, and subsequently

at a second current density for a second period of time to deposit a second amount of copper onto the first amount of copper such that the second amount of copper fills the recesses and forms a copper overburden extending over the dielectric layer, wherein the second current density is greater than the first current density and a majority of copper deposited onto the surface of the workpiece is deposited during the second time period; and

annealing the copper in the recesses and the copper overburden while the workpiece is within the tool at a predetermined temperature that is below about 300° C, wherein the annealing process occurs after plating copper into the recesses and before subsequent chemical mechanical polishing processes to increase the grain size of the copper and induce electromigration such that the conductivity of the deposited copper increases and electromigration resistance increases.

81. (Previously Presented) The process of Claim 80, wherein the second current density is applied immediately after the first period of time.

82. (Currently Amended) A process for electrochemical deposition of metal onto a surface of a semiconductor workpiece, the surface defining a plurality of recessed microstructures, the workpiece including at least one low-K dielectric layer, recesses in the low-K dielectric layer, a barrier layer on the low-K dielectric layer, and a copper seed layer on the barrier layer, the process comprising:

exposing a surface of the workpiece to a plating solution in a chamber in a tool, the plating solution including a principal metal species to be deposited, wherein the principal metal species to be deposited comprises copper;

applying plating power between the surface of the workpiece and an electrode electrically coupled to the plating solution to electrolytically deposit metal onto the surface, wherein plating power is applied

at a first current density for a first period of time to deposit a first layer of the metal onto the surface of the workpiece to at least partially fill the recessed microstructures, and subsequently

at a second current density for a second period of time to deposit a second layer of the metal onto the first layer of metal such that the second layer fills the recesses and forms a copper overburden over the low-K

dielectric layer, wherein the second current density is greater than the first current density; and

annealing the copper in the recesses and the copper overburden portion
~~while the workpiece is within the tool~~ at a predetermined temperature that is below a temperature at which the low-K dielectric layer would substantially degrade, wherein the annealing process occurs after plating copper into the recesses and before subsequent chemical mechanical polishing processes to increase the grain size of the copper ~~and induce electromigration~~ such that the conductivity of the deposited copper increases and electromigration resistance increases.

83. (Previously Presented) The process of Claim 82, wherein the second current density is applied immediately after the first period of time has elapsed.

84. (Currently Amended) A process for electrochemical deposition of metal onto a surface of a semiconductor workpiece having a dielectric layer, recesses in the dielectric layer, and a barrier layer on the dielectric layer, the process comprising:

applying a metal seed layer onto the barrier layer;

exposing the surface of the workpiece to a plating solution in a chamber of a tool, the plating solution including a principal metal species to be deposited, wherein the principal metal species to be deposited comprises copper;

applying plating power between the surface of the workpiece and an anode electrically coupled to the plating solution to electrolytically deposit copper into the recesses, wherein plating power is applied

at a first current density for a first period of time to deposit a first amount of copper onto the seed layer, and subsequently

at a second current density for a second period of time to deposit a second amount of copper onto the first amount of copper such that the second amount of copper fills the recesses and forms a copper overburden

extending over the dielectric layer, wherein the second current density is greater than the first current density; and
annealing the copper in the recesses ~~while the workpiece is within the tool and the copper overburden portion~~ in an elevated temperature annealing process at a predetermined temperature, wherein the annealing process occurs after plating copper into the recesses and before subsequent chemical mechanical polishing processes to increase the grain size of the copper ~~and induce electromigration such that the conductivity of the deposited copper increases and electromigration resistance increases~~.

85. (Currently Amended) A method of depositing a metal layer on a semiconductor wafer having a dielectric layer, recesses in the dielectric layer, and a barrier layer on the dielectric layer, the method comprising:

depositing a seed layer on the barrier layer;
immersing the wafer in an electrolytic solution containing metal ions, wherein the metal ions comprise copper, and wherein the electrolytic solution is in a chamber of a tool;
electrolytically depositing a first plated copper layer on the wafer by applying current at a first current density between the wafer and the solution;
after a first period of time during which the first plated copper layer has been formed, increasing the applied current to a second current density greater than the first current density to plate additional copper onto the first plated copper layer such that the additional copper fills the recesses and forms a copper overburden extending over the dielectric layer; and
annealing the copper in the recesses ~~and the copper overburden while the wafer is in the tool~~ in an elevated temperature annealing process at a predetermined temperature, wherein the annealing process occurs after plating copper into the recesses and before subsequent chemical mechanical polishing

processes to increase the grain size of the copper and induce electromigration such that the conductivity of the deposited copper increases and electromigration resistance increases.

86-106. (Cancelled)

107. (Previously Presented) The process of Claim 85, wherein the surface of the wafer defines a plurality of recessed microstructures, and the first current density and first period of time are selected to at least partially fill the recessed microstructures with the deposited metal.

108. (Previously Presented) The process of Claim 85, wherein metal deposited during the first time period has a grain size that is sufficiently small to fill the recessed microstructures and at least some of the recessed microstructures have a width of less than or equal to 0.3 micron.

109. (Previously Presented) The process of Claim 85, wherein the metal is annealed at a temperature of below about 250° C.

110. (Currently Amended) The process of Claim 85, wherein the first current density is about 3.2 mA/cm².

111. (Currently Amended) The process of Claim 85, wherein the second current density is about 20 mA/cm².

112. (Previously Presented) The process of Claim 68, wherein a ratio of the second current density to the first current density is about 6:1.

113. (Previously Presented) The process of Claim 85, wherein the first time period is about 30 seconds.

114. (Previously Presented) The process of Claim 85, wherein the metal is annealed at a temperature of below about 300° C.

115. (Previously Presented) The process of Claim 85, wherein metal is deposited at a higher rate during the second time period than during the first time period.

116. (Cancelled)

117. (Cancelled)

118. (New) A process for electrochemical deposition of copper onto a surface of a semiconductor workpiece in a plating tool, comprising:

providing a workpiece having a dielectric layer in which sub-micron recesses have been formed, a barrier layer on the dielectric layer, and a copper seed layer on the barrier layer;

electrolytically depositing copper onto the seed layer and into the recesses by applying a plating power at a first current density for a first period of time to deposit a first amount of copper into the recesses and subsequently applying plating power at a second current density higher than the first current density for a second period of time to deposit a second amount of copper that fills the recesses with copper and forms a copper overburden portion extending over the dielectric layer, wherein the electrolytically deposited copper has grain sizes substantially less than cross-sectional dimensions of the sub-micron recesses such that the electrolytically deposited copper has a high initial resistivity; and

annealing the copper in the recesses and in the copper overburden portion at an elevated temperature in an annealing process after depositing the second copper, but before removing the copper overburden portion, to increase grain sizes of the copper such that the resistivity of the electrolytically deposited copper decreases and the electromigration resistance increases.

119. (New) The process of claim 118 wherein the initial resistivity of the electrolytically deposited copper is approximately 1.725 M Ω ms-cm.

120. (New) The process of claim 118, further comprising removing the copper overburden portion from the workpiece by a chemical mechanical polishing process after annealing the electrolytically deposited copper.

121. (New) The process of claim 120, further comprising capping the copper in the recesses after removing the copper overburden portion.

122. (New) The process of claim 118 wherein the initial resistivity of the electrolytically deposited copper is greater than approximately 1.9 M Ω ms-cm.

123. (New) The process of claim 122, further comprising removing the copper overburden portion using a chemical mechanical polishing process after annealing the electrolytically deposited copper.

124. (New) The process of claim 123, further comprising capping the copper in the recesses after removing the copper overburden portion.

125. (New) The process of claim 118 wherein the initial sheet resistance of the electrolytically deposited copper is at least approximately 12.7 m Ω ms/sq.

126. (New) The process of claim 125, further comprising removing the copper overburden portion using a chemical mechanical polishing process after annealing the electrolytically deposited copper.

127. (New) The process of claim 125, further comprising capping the copper in the recesses after removing the copper overburden portion.